Operation of the HC55185 Ringing SLIC & TCM38C17 Evaluation Module

Application Note | October 2001 | AN9930.1

Functional Description

This application note is intended to supplement Texas Instruments TCM38C17 EVM Users Guide. The Users guide describes three ways of evaluating the circuits operation:

- Using a TMS320C5402 DSK
- Using an analog signal generator and the TCM38C17 in digital loopback
- Using a Wandel and Golterman (W&G) PCM4

A good understanding of the material in the Users Guide is a prerequisite to this application note. For a detailed engineering analysis of the HC55185 and TCM38C17 reference design, see application note AN9933.

This application note will evaluate the BASIC operation of the HC55185 (tests # 1- #3) and a system level evaluation (tests # 4 & #5) using the PCM4. For discussion purposes, the TCM38C17 EVM board will be referred to as the Mother Board and the HC55185 board will be referred to as the Daughter Board.

TCM38C17 Mother Board

The TCM38C17 Mother Board provides a way to evaluate the operation of Texas Instruments TCM38C17 Quad Combo and Intersil's HC55185 Ringing SLIC. The following steps, repeated here from the Users Guide, will configure the mother board for testing Channel 0 with the PCM4:

- Connect TCM38C17, HC55185 and PCM4 as shown in Figure 1.
- Configure the PCM4 general parameters per Table 1.
- Configure dipswitch SW7 as shown in Figure 2 for Channel 0 selected.
- Verify jumper JP1: Pin 2 shorted to Pin 3 (FPGA prom installed)
- Verify jumper JP2: Open (CODEC output gain setting set by SLIC EVM)
- Verify jumper JP6: Open (external loopback not configured)
- Verify jumper JP7: Shorted (analog and digital grounds connected)
- Verify jumper JP8: Open (power supplied by external power supplies)
- Connect the external supplies to the Mother Board as shown in Table 2. NOTE: The Daughter Board gets its power from the Mother Board.

Evaluation of channels 1-3 is accomplished by moving the daughter board to the desired channel and configuring SW7 to select that channel. SW7 selects the channel of the TCM38C17 that receives conversion data first. This will enable proper operation of the PCM4 once the transmit and receive channels are set to channel zero.

Daughter Board

The HC55185EVAL2 REV A evaluation board is configured to match a 600Ω line impedance, have a Ring Trip Threshold of 76mA, a Switch Hook Threshold of 12mA, Loop Current Limit of 24.6mA and a Transient Current Limit of 95mA.

For evaluation of the programmability of the HC55185 family, reference the data sheet for calculation of external components.

The daughter board is equipped with five (5) Single Pole Double Throw (SPDT) switches and one normally open push button switch. The switches labeled E0, F0, F1, and F2 control the logic state HC55185 and the switch labeled BSEL selects between the high battery and low battery. When BSEL is a logic high the high battery is selected and when low the low battery is selected. The push button ($\overline{SWC}$) controls the operation of the uncommitted switch. Press the button and the uncommitted switch is closed. TP1 and TP2 (located near the center of the daughter board, Figure 4) provide a direct connection to the terminals of the uncommitted switch.

Features of the HC55185EVAL2 Daughter Board

- Toggle Switch Programming for Logic States
- Monitoring of Switch Hook, Ground Key, Ring Trip and Thermal Shutdown (Alarm) via On Board LEDs
- Selectable Battery Operation
- Easy Balanced Ringing Evaluation
- Easy Evaluation of Uncommitted Switch

Getting Started

Verify that the HC55185 is oriented in its socket correctly. Correct orientation is with pin 1 lined up with the pin 1 indicator on the board (Figure 4). (Reference the data sheet for device pinout.)

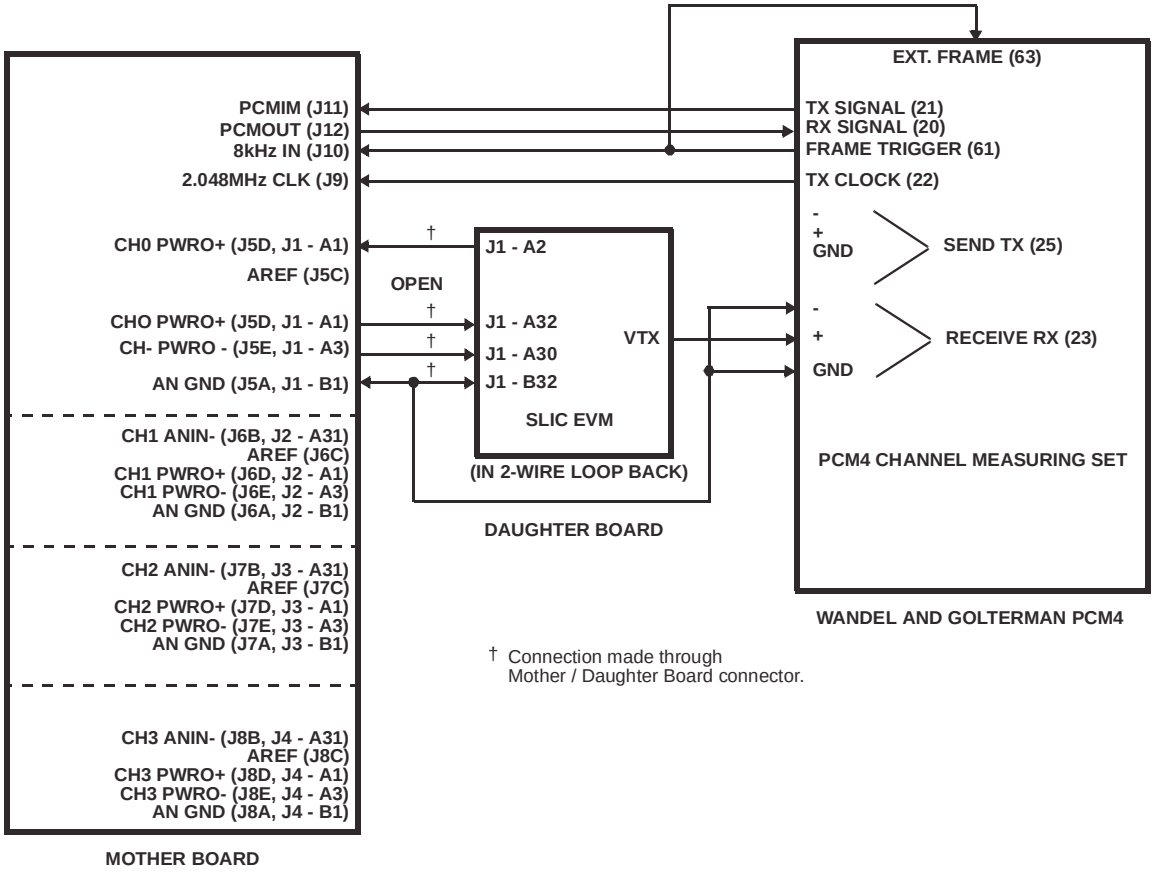

FIGURE 1. TCM38C17 CONNECTIONS TO PCM4 WITH HC55185 EVM CONNECTED

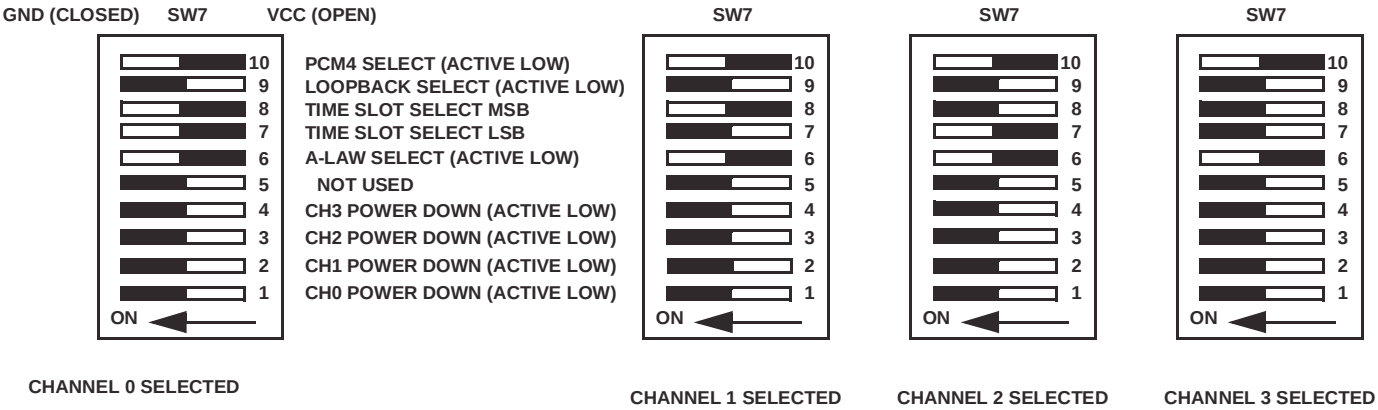

FIGURE 2. MOTHER BOARD SW7 DEFINITIONS AND CHANNEL SELECTION

TABLE 1. GENERAL PARAMETER SETTINGS IN THE PCM4

GENERAL PARAMETER	SETTING	ITEM NUMBER
(1) Digital Configuration		
General configuration	TX/RX 2M/2Mbits/s selected	11
Digital Loop (D - A)	2Mbits/s/all TS	21
(2) Frame Selection		
TX frame type	All 32 TS teleph	14
RX frame type	All 32 TS teleph	24
CRC-4 Multiframe	Off	31
(3) Digital TX Interface		
Line Code	75Ω unbalanced	13
Output Impedance	NRZ	22
Clock	Int. 2048 kHz	31
(4) Digital RX Interface		
Line Code	NRZ	13
Input Impedance	> 3kΩ	22
(5) Digital Words in TX Frame		
Frame Words	Reset to standard values	11
Send Signal	In select channels	21
(6) TX Error Insertion	Off	11
(7) PCM Coding		
TX Encoding Law	Must match switch S7-6 on TCM38C17 EVM. Default setting on EVM is A-law	11 to match EVM default
RX Encoding Law	Must match encoding law	21 to match EVM default
(8) Scanner Parameter		
VF-Input no.	1	11
VF-Output no.	1	21
(9) Special Parameter		
Level Display	dBm0	11
Two wire Term.	Infinite	13
Digital Channel no.	Time Slot	16

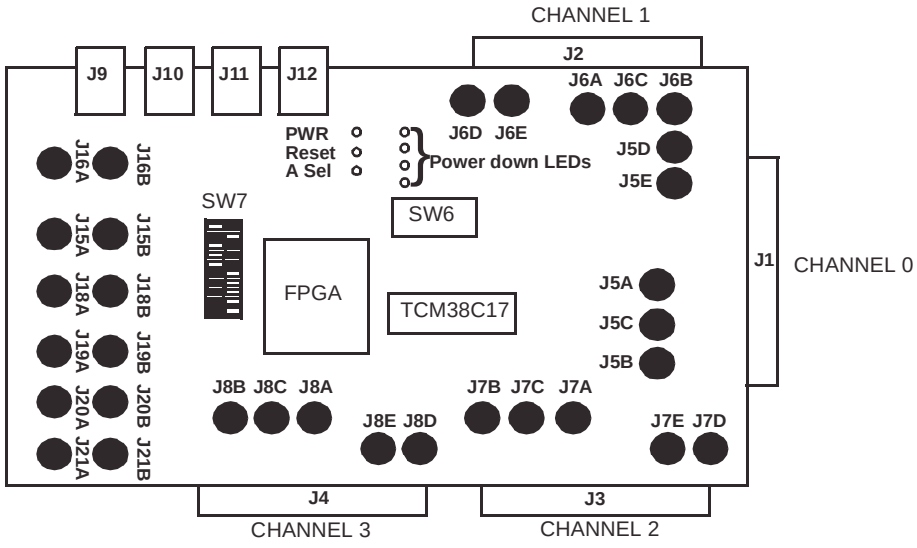

FIGURE 3. MOTHER BOARD LAYOUT

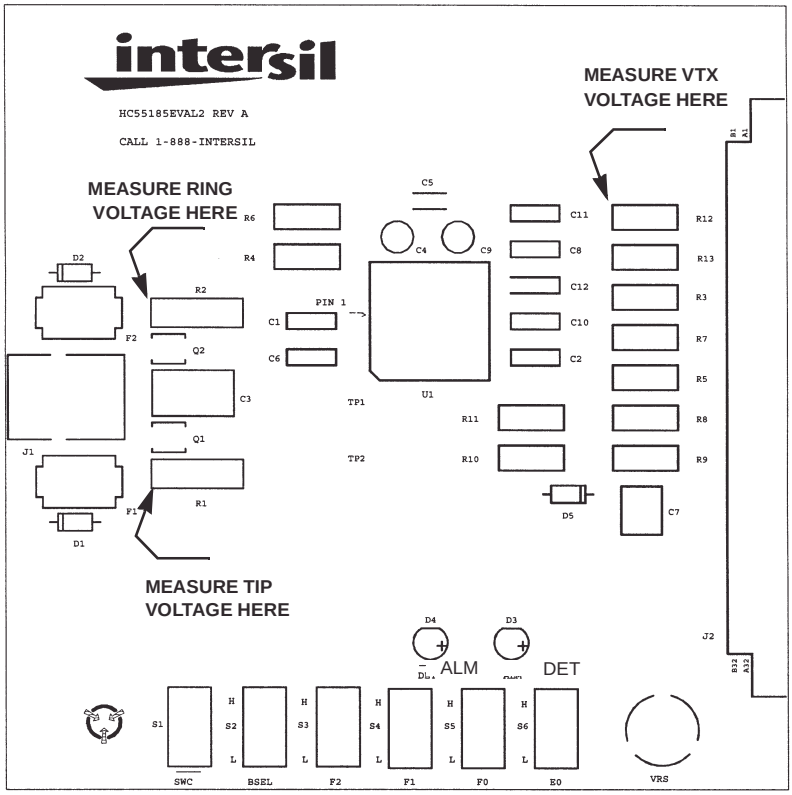

FIGURE 4. DAUGHTER BOARD LAYOUT

TABLE 2. POWER SUPPLY INTERFACE CONNECTIONS

POWER	CONNECTOR REFERENCE DESIGNATOR	REQUIRED BY
+5V Digital	J16A	TCM38C17 and Digital Circuits
Digital Ground	J16B	TCM38C17 and Digital Circuits
+5V Analog	J15A	TCM38C17 and SLICs
Analog Ground	J15B	TCM38C17 and SLICs
-24V (V_{BL})	J18A	SLICs
(V_{BL}) Ground	J18B	SLICs
-48, -100 (V_{BH})	J19A	SLICs
-48, -100V (V_{BH}) Ground	J19B	SLICs

Operation & Performance of the Daughter Board

The operation and performance of the daughter board will be verified in two ways. The first will evaluate the operation of the daughter board itself, and the second will evaluate the operation of the daughter board and mother board in a system configuration.

Verifying Basic SLIC Operation

The operation of the Customer Evaluation Board with it's sample part can be verified by performing the following tests:

1. Normal Loop Feed Verification
   Forward Active State, On Hook
   Forward Active State, Off Hook
   Reverse Active State, On Hook
   Reverse Active State, Off Hook
   Tip Open State, Ground Key Test
   Forward Loopback State
2. Gain Verification
   4-wire to 2-wire and 4-wire to 4-wire
3. Ringing Verification
4. Variable Gain/Frequency (system test)
5. Total Distortion (system test)

Test # 1 Normal Loop Feed Verification

This test verifies the correct tip and ring voltages in both onhook and offhook forward active and reverse active states. Loop current and ground key detect are also verified via the onboard $\overline{\text{DET}}$ LED.

Discussion

The HC55185 is designed to have its most positive 2-wire terminal (tip in the forward active state and ring in the reverse active state) fixed at a set voltage. The most negative 2-wire terminal voltage is dependent upon the load across tip and ring and the programmable current limit.

Loop supervision is provided by either the switch hook detector (E0 = 1) or the ground key detector (E0 = 0). The device may be operated from either high or low battery for on-hook transmission, during ringing and low battery for loop feed.

When operating from the high battery, the DC voltages at Tip and Ring are MTU compliant. The typical Tip voltage is -4V and the Ring voltage is a function of the battery voltage for battery voltages less than -60V as shown in Equation 1.

$$V_{RING} = V_{BH} + 4 \quad \text{(EQ. 1)}$$

Most applications will operate the device from low battery while off hook. The DC feed characteristic of the device will drive Tip and Ring towards half battery to regulate the DC loop current. For light loads, Tip will be near -4V and Ring will be near V_{VBL} + 4V. The following diagram shows the DC feed characteristic.

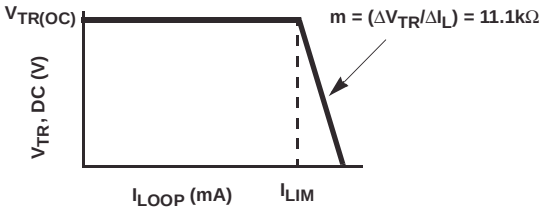

FIGURE 5. DC FEED CHARACTERISTIC

The point on the y-axis labeled $V_{TR(OC)}$ is the open circuit Tip to Ring voltage and is defined by the feed battery voltage.

$$V_{TR(OC)} = |V_{BL}| - 8 \quad \text{(EQ. 2)}$$

The Ground Key detector operation is verified by configuring the HC55185 in the tip open state and grounding the ring pin. Grounding the ring pin results in a current that triggers an internal detector that pulls the output of $\overline{\text{DET}}$ low, illuminating the LED through the +5V supply.

The Forward Loop Back mode provides test capability for the device. An internal signal path is enabled allowing for both DC and AC verification. The internal 600Ω terminating resistor has a tolerance of ±20%. The device is intended to operate from only the low battery during this mode.

When the forward loop back mode is initiated internal switches connect a 600Ω load across the outputs of the Tip and Ring amplifiers as shown in Figure 6.

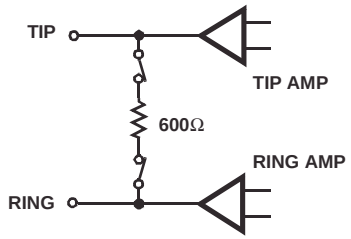

FIGURE 6. FORWARD LOOP BACK INTERNAL TERMINATION

DC Verification

When the internal signal path is provided, DC current will flow from Tip to Ring. The DC current will force $\overline{DET}$ low, indicating the presence of loop current. In addition, the $\overline{ALM}$ output will also go low. This does not indicate a thermal alarm condition.

Setup (Tip and Ring Voltages)

1. Configure SW7 on the mother board for testing channel 0 with the PCM4. Reference Figure 2.
2. Connect daughter board to port J1 (Channel 0) of mother board Reference Figure 3.
3. Apply power to the system (apply 5V then -24V and -48V) and turn on the PCM4.
4. Verify supply voltages V_{BH} (J19A) = -48V, V_{BL} (J18A) = -24V and V_{CC} (J15A, J16A) = +5V.
5. Set S2, on the daughter board, to the high battery position BSEL = 1 (switch lever towards top of board). Reference Figure 4.
6. All of the channel power-down LED's will be illuminated along with the PWR LED and the A SEL LED (Figure 3). **This test will be preformed with all channel from the mother board in the power down condition (all LED's illuminated).**
7. Configure the SLIC to be in the Forward Active State (F2 = 0, F1 = 0, F0 = 1, E0 = 1, BSEL = 1).
8. Measure the tip and ring voltages (reference Figure 4) on the left side of resistors R1 and R2 with respect to ground and compare to those in Table 3 (onhook).
9. Terminate TIP and RING with a 600Ω load via the RJ11 jack.
10. Measure tip and ring voltages with respect to ground and compare to those in Table 3 (offhook 600Ω).
11. Configure the SLIC to be in the Reverse Active State (F2 = 0, F1 = 1, F0 = 1, E0 = 1, BSEL = 1).
12. Disconnect the 600Ω load from across tip and ring.
13. Repeat steps 8 through 10.

TABLE 3. TIP AND RING VOLTAGES

LOGIC STATE	R_L (Ω)	TIP VOLTAGE REFERENCED TO GND	RING VOLTAGE REFERENCED TO GND
Forward Active V_{BH} = -48V V_{BL} = -24V V_{CC} = +5V	Onhook	-3.5 — -4.5	-37.0 — -44.0
	Offhook 600Ω	-13.5 — -17.0	-28.0 — -32.0
Reverse Active V_{BH} = -48V V_{BL} = -24V V_{CC} = +5V	Onhook	-38.0 — -44	-3.5 — -4.5
	Offhook 600Ω	-28.0 — -32.0	-13.5 — -17.0

Verification of Switch Hook Detect

1. With the SLIC in the forward active state, the $\overline{DET}$ LED is on when tip and ring are terminated with 600Ω and off when tip and ring are an open circuit.

Verification of Ground Key Detect

1. Configure the SLIC to be in the Tip Open State (F2 = 1, F1 = 1, F0 = 0, E0 = 0, BSEL = 1).
2. The $\overline{DET}$ LED is on when ring is shorted to ground and off when ring is an open circuit.

Verification of Forward Loopback

1. Set S2, on the daughter board, to the low battery position BSEL = 0 (switch lever towards bottom of board). Reference Figure 4. (Damage to SLIC can occur in high battery operation.)
2. Configure the SLIC to be in the Forward Loopback State (F2 = 1, F1 = 0, F0 = 1, E0 = 1, BSEL = 0).

The $\overline{DET}$ and $\overline{ALM}$ LEDs are on when in the Forward Loopback mode.

Test # 2 Gain Verification

This test will verify the SLIC is operating properly and that the 4-wire to 2-wire gain (Equation 3) is equal to -1.0 (0.0dB). +PWRO = V_{RX}

$$G_{4\text{-}2} = \frac{V_{2W}}{V_{RX}} = -2\frac{Z_L}{Z_L + Z_O + 2_{RP}} \quad \text{(EQ. 3)}$$

The programmable 2-wire to 4-wire transmission gain will also be verified by measuring the SLIC's 4-wire to 4-wire gain. The 4-wire to 4-wire gain is equal to the 2-wire to 4-wire gain as shown in Equation 4.)

$$G_{4\text{-}4} = \frac{V_{TX}}{V_{RX}} = G_{2\text{-}4} = -\frac{Z_O}{(Z_L + 2R_P + Z_O)} \quad \text{(EQ. 4)}$$

Discussion

When tip and ring are terminated with 600Ω load, the SLIC will exhibit unity gain from the 4-wire VRX input pin to across the 2-wire tip and ring pins (V_{TR}). When an open circuit exists, a mismatch occurs and the tip to ring voltage doubles.

An easy way to measure the 2-wire to 4-wire transmit gain, without a floating signal generator on the 2-wire side, is to use the signal from the PCM4 through the mother board and measure the 4-wire to 4-wire gain. Given that the 4-wire to 2-wire gain is approximately one, it follows that the 2-wire to 4-wire transmission gain is also approximately equal to the 4-wire to 4-wire gain. The dB 4w to 4w gain is calculated in Equation 5.

$$dB_{4W-4W} = 20\log\frac{V_{TX}}{V_{RX}} \quad \text{(EQ. 5)}$$

Setup (4-wire to 2-wire Gain) Test #2a

If previous test was Test #1, skip to step 7.

1. Configure mother board for testing channel 0 with the PCM4. Reference Figure 2.
2. Connect daughter board to port J1 (Channel 0) of mother board Reference Figure 3.

3. Apply power to the system (apply 5V then -24V and -48V) and turn on the PCM4.
4. Verify supply voltages V_{BH} (J19A) = -48V, V_{BL} (J18A) = -24V and V_{CC} (J15A, J16A) = +5V.
5. Set S2, on the daughter board, to the high battery position BSEL = 1 (switch lever towards top of board). Reference Figure 4.
6. All of the channel power-down LED's will be illuminated along with the PWR LED and the A SEL LED (Figure 3).
7. Press the TCM38C17 reset switch (SW6). The channel power-down LED's will turn off.
8. Configure the PCM4 for the MODE A11 test. Set the level to 0dBm0. Set PCM4 to D-A. Set the frequency to 1004Hz. This will provide a 1kHz 1Vrms signal at the VRX input to the SLIC.
9. Configure the SLIC to be in the Forward Active State (F2 = 0, F1 = 0, F0 = 1, E0 = 1, BSEL = 1).
10. Terminate TIP and RING with a 600Ω load via the RJ11 jack.
11. Connect an AC voltmeter across tip and ring.

Verification

1. Tip to ring AC voltage of approximately $1V_{RMS}$ when terminated with a 600Ω load. The dB (A_{4-2}) gain is approximately 0dB.
2. Tip to ring AC voltage of approximately $2V_{RMS}$ when not terminated. The dB (A_{4-2}) gain is approximately 6dB.
3. Configure the SLIC to be in the Reverse Active state (F2 = 0, F1 = 1, F0 = 1, E0 = 1, BSEL = 1) and repeat steps 1 and 2 above .

Setup (2-wire to 4-wire Gain) Test #2b

If previous test was test #2a, skip to step 9.

1. Configure mother board for testing channel 0 with the PCM4. Reference Figure 2.
2. Connect daughter board to port J1 (Channel 0) of mother board. Reference Figure 3.
3. Apply power to the system (apply 5V then -24V and -48V) and turn on the PCM4.
4. Verify supply voltages V_{BH} (J19A) = -48V, V_{BL} (J18A) = -24V and V_{CC} (J15A, J16A) = +5V.
5. Set S2, on the daughter board, to the high battery position BSEL = 1 (switch lever towards top of board). Reference Figure 4.
6. All of the channel power-down LED's will be illuminated along with the PWR LED and the A SEL LED (Figure 3).
7. Press the TCM38C17 reset switch (SW6). The channel power-down LED's will turn off.
8. Configure the PCM4 for the MODE A11 test. Set the level to 0dBm0. Set PCM4 to D-A. Set the frequency to 1004Hz. This will provide a 1kHz 1Vrms signal at the VRX input to the SLIC.
9. Configure the SLIC to be in the Forward Active State (F2 = 0, F1 = 0, F0 = 1, E0 = 1, BSEL = 1).
10. Terminate TIP and RING with a 600Ω load via the RJ11 jack.
11. Connect an AC voltmeter, referenced to ground, to the left hand side of resistor R12 to measure the voltage at VTX (reference Figure 4).

Verification

1. VTX voltage of approximately $0.416V_{RMS}$. The dB (A_{2-4}) gain is approximately -7.6dB.
2. Configure the SLIC to be in the Reverse Active state (F2 = 0, F1 = 1, F0 = 1, E0 = 1, BSEL = 1) and repeat step 1 above.

Test # 3 Ring Trip Verification

This test will verify the ringing function of the HC55185. A telephone is the only additional hardware required to complete this test.

Discussion

The HC55185 provides linear amplification to support a variety of ringing waveforms. A programmable ring trip function provides loop supervision and auto disconnect upon ring trip. The device is designed to operate from the high battery during this mode.

Architecture

The device provides linear amplification to the signal applied to the ringing input, V_{RS}. The differential ringing gain of the device is 80V/V. The circuit model for the ringing path is shown in Figure 7.

The voltage gain from the VRS input to the Tip output is 40V/V. The resistor ratio provides a gain of 8 and the current mirror provides a gain of 5. The voltage gain from the VRS input to the Ring output is -40V/V. The equations for the Tip and Ring outputs during ringing are given in Equations 6 and 7.

$$V_T = \frac{V_{BH}}{2} + (40 \times VRS) \quad \text{(EQ. 6)}$$

$$V_R = \frac{V_{BH}}{2} - (40 \times VRS) \quad \text{(EQ. 7)}$$

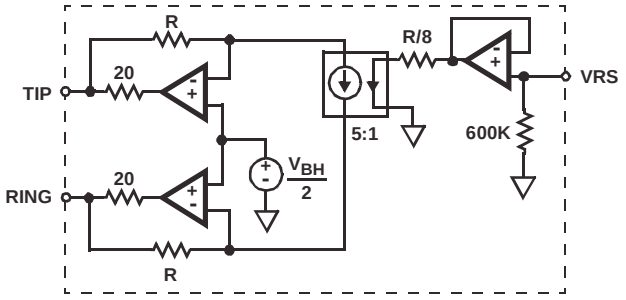

FIGURE 7. LINEAR RINGING MODEL

When the input signal at VRS is zero, the Tip and Ring amplifier outputs are centered at half battery. The device provides auto centering for easy implementation of sinusoidal ringing waveforms. Both AC and DC control of the Tip and Ring outputs is available during ringing. This feature allows for DC offsets as part of the ringing waveform.

Ringing Input

The ringing input, V_{RS}, is a high impedance input. The high impedance allows the use of low value capacitors for AC coupling the ring signal. The V_{RS} input is enabled only during the ringing mode, therefore a free running oscillator may be connected to VRS at all times.

When operating from a battery of -100V, each amplifier, Tip and Ring, will swing a maximum of $95V_{P-P}$. Hence, the maximum signal swing at VRS to achieve full scale ringing is approximately $2.4V_{P-P}$. The low signal levels are compatible with the output voltage range of the CODEC. The digital nature of the CODEC ideally suits it for the function of programmable ringing generator.

Setup

If previous test was either test #1 or #3, skip to step 8.
If previous test was test #2a or 2b, skip to step 6.

1. Configure mother board for testing channel 0 with the PCM4. Reference Figure 2.
2. Connect daughter board to port J1 (Channel 0) of mother board Reference Figure 3.
3. Apply power to the system (apply 5V then -24V and -100V) and turn on the PCM4.
4. Verify supply voltages V_{BH} (J19A) = -48V, V_{BL} (J18A) = -24V and V_{CC} (J15A, J16A) = +5V.
5. Set S2, on the daughter board, to the high battery position BSEL = 1 (switch lever towards top of board). Reference Figure 4.
6. Turn off power to the system to reset the mother board so all channels are in power-down state after power is applied.
7. All of the channel power-down LED's will be illuminated along with the PWR LED and the A SEL LED (Figure 3). **This test will be preformed with all channel from the mother board in the power down condition (all LED's illuminated).**
8. Connect the telephone across tip and ring via the RJ11 jack on the daughter board.
9. Connect a 20Hz sine wave 2.4Vpp signal to the VRS BNC located in the right hand side of the daughter board.
10. Set the V_{BH} power supply to -100V.
11. Configure the SLIC to be in the Ringing State (F2 = 1, F1 = 0, F0 = 0, E0 = 1, BSEL = 1).

Verification

1. The phone should now be ringing. Lift the phone off hook and the ringing should stop. Replace the phone on hook and reset the logic switches to Forward Active State (F2=0, F1=0, F0=1) and back to Ringing State (F2=1, F1=0, F0=0) and the phone will ring again.

Test # 4 Variable Gain / Frequency

This test will configure the HC55185 in the loopback mode and evaluate the TCM38C17 and the HC55185's AC performance across frequency.

Discussion

Most of the SLICs in the HC55185 family feature 2-Wire loopback testing. During the 2-wire loopback test, a 600Ω internal resistor is switched across the tip and ring terminals of the SLIC. This allows the $\overline{DET}$ function and the 4-wire to 4-wire AC transmission, right up to the subscriber loop, to be tested.

Setup

If previous test was either test #2a or 2b, skip to step 8.
If previous test was either test #1 or #3, skip to step 6.

1. Configure mother board for testing channel 0 with the PCM4. Reference Figure 2.
2. Connect daughter board to port J1 of mother board Reference Figure 3.
3. Apply power to the system (apply 5V then -24V and -48V) and turn on the PCM4.
4. Verify supply voltages V_{BH} (J19A) = -48V, V_{BL} (J18A) = -24V and V_{CC} (J15A, J16A) = +5V.
5. All of the channel power-down LED's will be illuminated along with the PWR LED and the A SEL LED (Figure 3).
6. Press the TCM38C17 reset switch (SW6). The channel power-down LED's will turn off.
7. For safety reasons, set / verify the VBH supply is -48V.
8. Set S2, on the daughter board, to the low battery position BSEL = 0 (switch lever towards bottom of board). Reference Figure 4. (Damage to SLIC can occur in high battery operation.)
9. Configure the SLIC to be in the Forward Loopback State (F2 = 1, F1 = 0, F0 = 1, E0 = 1, BSEL = 0).
10. Configure the PCM4 for the MODE A 33 test. Set PCM4 to D-A, SWP/S (single sweep). Press start to test part.

Verification

Compare results to Figure 8.

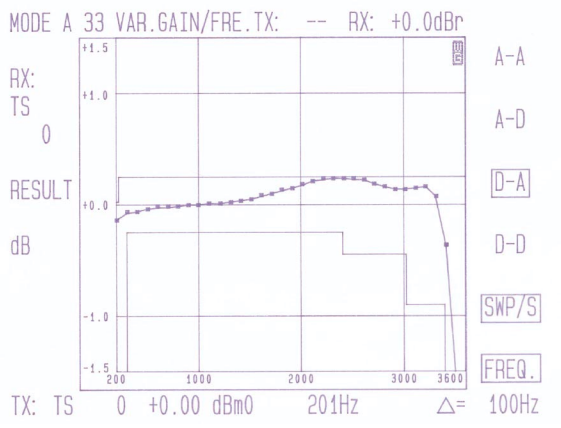

FIGURE 8. VARIABLE GAIN vs FREQUENCY

Test # 5 Total Distortion

This test will configure the HC55185 in the loopback mode and evaluate the TCM38C17 and the HC55185's Total Distortion.

Discussion

Most of the SLICs in the HC55185 family feature 2-Wire loopback testing. During the 2-wire loopback test, a 600Ω internal resistor is switched across the tip and ring terminals of the SLIC. This allows the $\overline{\text{DET}}$ function and the 4-wire to 4-wire AC transmission, right up to the subscriber loop, to be tested.

Setup

If previous test was either test #2a or #2b, skip to step 8.
If previous test was either test #1 ,#3 , skip to step 6.
If previous test was test #4, skip to step 10.

1. Configure mother board for testing channel 0 with the PCM4. Reference Figure 2.
2. Connect daughter board to port J1 of mother board Reference Figure 3.
3. Apply power to the system (apply 5V then -24V and -48V) and turn on the PCM4.
4. Verify supply voltages V_{BH} (J19A) = -48V, V_{BL} (J18A) = -24V and V_{CC} (J15A, J16A) = +5V.
5. All of the channel power-down LED's will be illuminated along with the PWR LED and the A SEL LED (Figure 3).
6. Press the TCM38C17 reset switch (SW6). The channel power-down LED's will turn off.
7. For safety reasons, set / verify the VBH supply is -48V.
8. Set S2, on the daughter board, to the low battery position BSEL = 0 (switch lever towards bottom of board). Reference Figure 4. (Damage to SLIC can occur in high battery operation.)
9. Configure the SLIC to be in the Forward Loopback State (F2 = 1, F1 = 0, F0 = 1, E0 = 1, BSEL = 0).
10. Configure the PCM4 for the MODE A 51 test. Set PCM4 to D-A, SWP/S (single sweep). Press start to test part.

Verification

Compare results to that shown in Figure 9.

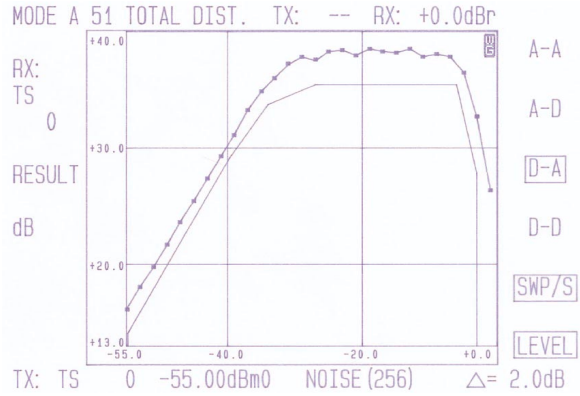

FIGURE 9. TOTAL DISTORTION

Demo Board Schematic

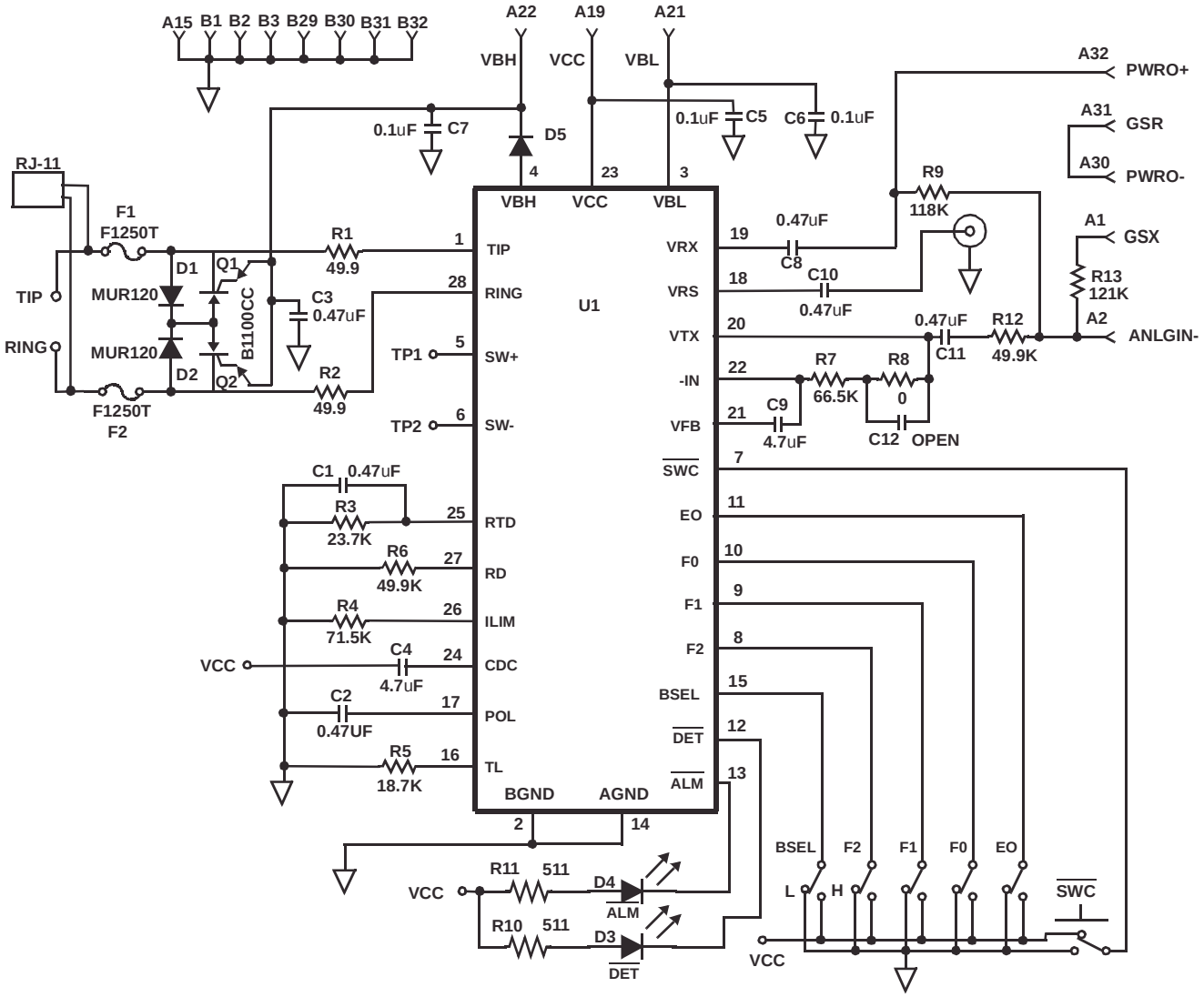

FIGURE 10. HC55185 DEMO DAUGHTER BOARD SCHEMATIC

TABLE 4. BASIC APPLICATION CIRCUIT COMPONENT LIST

COMPONENT	VALUE	TOLERANCE	RATING
U1 - SLIC	HC55185	N/A	N/A
Q1, Q2 BATTRIX	B1100CC	N/A	N/A
R1, R2 (Line feed resistors)	49.9Ω	Matched 1%	2.0W
R3	23.7kΩ	1%	1/16W
R4	71.5kΩ	1%	1/16W
R5	18.7kΩ	1%	1/16W
R6	49.9kΩ	1%	1/16W
R7	66.5kΩ	1%	1/16W
R8	0Ω	1%	1/16W
R9	118Ω	1%	1/4W
R10	511Ω	1%	1/16W
R11	511Ω	1%	1/16W
R12	49.9kΩ	1%	1/16W
R13	121kΩ	1%	1/16W
C1, C2, C8, C10, C11	0.47µF	20%	50V
C3	0.47µF	20%	100V
C4, C9	4.7µF	10%	50V
C5, C6	0.1µF	20%	50V
C7	0.1µF	20%	100V
C12	Open		
$\overline{DET}$ and $\overline{ALM}$ LEDs	Red	-	-
D1, D2	MUR120		
F1, F2	F1250T		
D5, Recommended if the V_{BL} supply is not derived from the V_{BH} supply.	1N4004	-	-

Design Parameters: Ring Trip Threshold = 76mApeak, Switch Hook Threshold = 12mA, Loop Current Limit = 24.6mA, Synthesize Device Impedance = (3*66.5KΩ/400 = 498.8Ω, with 49.9Ω protection resistors, impedance across Tip and Ring terminals = 599Ω . Transient current limit = 95mA.

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
7585 Irvine Center Drive
Suite 100
Irvine, CA 92618
TEL: (949) 341-7000
FAX: (949) 341-7123

Intersil Corporation
2401 Palm Bay Rd.
Palm Bay, FL 32905
TEL: (321) 724-7000
FAX: (321) 724-7946

EUROPE

Intersil Europe Sarl
Ave. C - F Ramuz 43
CH-1009 Pully
Switzerland
TEL: +41 21 7293637
FAX: +41 21 7293684

ASIA

Intersil Corporation
Unit 1804 18/F Guangdong Water Building
83 Austin Road
TST, Kowloon Hong Kong
TEL: +852 2723 6339
FAX: +852 2730 1433